Serial No.: 10/791,130
Group Art Unit: 2829

REMARKS

Claim Rejections - 35 USC §102

Claims 1-3, 6-7, 10-13, 16-17 and 20 are rejected under 35 U.S.C. §102(e) as being anticipated by Cowan (U.S. Patent No. 6,605,951, hereinafter "Cowan").

Cowan provides an interconnector and method for connecting probes to a die for functional analysis. Interconnectors are placed on a die containing a semiconductor device or integrated circuit that is to be tested or analyzed. Each interconnector includes a bump contact for contacting a bond pad of the die, and a probe pad at a position spaced from the bump contact. An interconnector connects the bump contact and the probe pad. The interconnector is attached to the die with the bump contact in electrical contact with a respective die bond pad and with the probe pad extending beyond an exterior peripheral edge of the die. Probes apply signals or power to the probe pad, and those signals and power are applied to the semiconductor device or integrated circuit for die test or analysis.

Regarding independent claims 1, 6, 11, and 16, the Applicants respectfully traverse the rejections of these claims since the Applicants' claimed combinations, as exemplified in claim 1, includes the limitation not disclosed in Cowan of:

"providing a plurality of opposing electrical contacts"

The Examiner states in the Office Action dated September 28, 2005:

> "providing a plurality of opposing electrical contacts (bump contacts 62)"

However, Cowan does not disclose opposing electrical contacts, but at column 5, lines 18–31, states:

> "A...bump contact 62 is mounted on the top surface 48...of the tape 46...The bump contact 62...attach[es] itself to...the die 22...as shown in FIG. 3." [deletions and underlining for clarity]

Thus, as described and as shown in FIG. 3, while the tapes 46 may be considered to face one another and thus be "opposing", the bump contacts 62 both face in the same

(upward) direction toward the die 22. The bump contacts 62 are thus disposed parallel to one another, not opposing. Thus Cowan does not disclose a plurality of opposing electrical contacts as claimed in claims 1, 6, 11, and 16.

The Applicants additionally traverse the rejections of claims 1, 6, 11, and 16 since the Applicants' claimed combinations, as exemplified in claim 1, includes the limitation not disclosed in Cowan of:

> "configuring the electrical contacts...such that any one electrical contact may contact more than one conductor in the sample" [deletions for clarity]

The Examiner states in the Office Action:

> "configuring the electrical contacts (62)...such that any one electrical contact may contact more than one conductor in the sample" [deletions for clarity]

However, Cowan states that each bump contact 22 makes a single electrical connection to the die 22:

> "Preferably, the interconnector 11 is...in the form of a single strip for making a single electrical connection between the die 22 and the probe 16." (column 5, lines 36–39) [deletions and underlining for clarity]

> "the interconnector 11...connects to a single bond pad 66" (column 5, lines 60–61) [deletions and underlining for clarity]

> "Bump contacts 62 on the interconnector pad 68 are formed at predetermined positions to line up with and contact the bond pads 66 (FIG. 3)" (column 6, lines 1–3) [deletions and underlining for clarity]

> "to hold each bump contact 62 in contact with a bond pad 66" (column 7, lines 9–10) [deletions and underlining for clarity]

Thus Cowan does not disclose configuring the electrical contacts such that any one electrical contact may contact more than one conductor in the sample as claimed in claims 1, 6, 11, and 16.

Based on the above, it is respectfully submitted that independent claims 1, 6, 11, and 16, and the respective claims 2–5, 7–10, 12–15, and 17–20 depending directly or indirectly respectively therefrom, are allowable under 35 USC §102(e) because:

> "Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, *arranged as in the claim.*" [emphasis added] Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co. (730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing Connell v. Sears, Roebuck & Co., 722 F.2d 1542, 220 USPQ 193 (Fed Cir. 1983)))

Withdrawal of the rejections is therefore respectfully requested.

Regarding claims 2, 3, 7, 10, 12, 13, 17, and 20, these dependent claims each depend directly or indirectly from respective independent claims 1, 6, 11, and 16 and are believed to be allowable since they contain all the limitations set forth in the independent claims from which they respectively depend and additionally claim non-obvious combinations thereof. Allowance of claims 2, 3, 7, 10, 12, 13, 17, and 20 is therefore respectfully requested because of Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co. and the other cases cited therewith, *supra*.

Claim Rejections - 35 USC §103

Claims 4-5, 8-9, 14-15 and 18-19 are rejected under 35 U.S.C. §103(a) as being unpatentable over Cowan (U.S. Patent No. 6,605,951 B1, hereinafter "Cowan") in view of Takao (U.S. Patent No. 6,639,417 B2, hereinafter "Takao").

Cowan was previously summarized above.

Takao provides a semiconductor parametric testing apparatus for testing the parameters of a designated semiconductor die. The testing includes designating a die and module on each wafer at which a test should be paused, and pausing a test at the preselected die and module on each wafer. An operator can interactively determine the contents of a test after a pause and start a subprogram for performing another test, for more easily and quickly discovering the cause of a failure.

Regarding claims 4, 8, 14, and 18, these dependent claims each depend from respective independent claims 1, 6, 11, and 16, and are believed to be allowable since they contain all the limitations set forth therein and additionally claim non-obvious combinations thereof. Allowance of claims 4, 8, 14, and 18 is therefore respectfully requested on this

ground as well because of Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co. and the other cases cited therewith, *supra*.

The Applicants also respectfully traverse the rejections of claims 4, 8, 14, and 18 on the grounds that the Applicants' claimed combinations would be patentable over Cowan in view of Takao since the Applicants' claimed combinations, as exemplified in claim 4, includes the limitation not disclosed in either Cowan or Takao of:

"providing a parametric test structure for testing the opposing contacts"

The Examiner states in the Office Action:

> "...Cowan...does not disclose a parametric test structure as claimed. Takao discloses [Fig. 6] a tester (tester 3) for failure analysis of small contacts in integrated circuits (IC wafer 2), comprising: a plurality of opposing electrical contact arrays (wafer prober 5) and a parametric test structure (parametric testing system 1) for testing the opposing contacts." [deletions for clarity]

However, Takao does not teach or suggest "a plurality of opposing electrical contact arrays (wafer prober 5)", but at column 1, lines 48–61 only discloses the wafer prober 5 as:

> "The definitions of terms used in this specification are as follows...The wafer prober 5 puts its probe on each module 21...The wafer prober 5 is connected physically and electrically to the wafer 2" [deletions for clarity]

The above shows that Takao does not teach or suggest opposing electrical contacts, and could not provide this teaching for a combination with Cowan.

Further, Takao teaches and suggests nothing about "a parametric test structure (parametric testing system 1) for testing the opposing contacts", as stated by the Examiner.

First, there is no disclosure or suggestion in Takao for "opposing contacts", as just explained above, so there is no corresponding structure disclosed for testing any such undisclosed opposing contacts.

Secondly, the "parametric testing system 1" of Takao is a system for testing the parameters of a semiconductor die, not for testing the contacts of a die tester, as explained in Takao column 1, lines 8–13:

> "The present invention relates...to a semiconductor parametric testing apparatus for measuring several parameters for semiconductors on a wafer and

> testing them in, for example, the process for manufacturing semiconductor integrated circuits" [deletions and underlining for clarity]

The parametric test structure of the present invention (specimen slice 302 as described on Specification page 9, line 2), however, is configured for testing opposing upper and lower tester micro-contacts (i.e., the Applicants' contacts 304 and 306) not for testing a semiconductor die. The parametric testing apparatus of Takao is incapable of testing opposing upper and lower tester micro-contacts (present invention). Therefore, as the above shows, Takao does not teach or suggest "providing a parametric test structure for testing the opposing contacts" of the tester of the present invention, and could not provide such a teaching for a combination with Cowan.

Accordingly, neither Cowan nor Takao provides a parametric test structure for testing the opposing contacts, and there is thus no teaching, suggestion, or motivation in either of these references for the combination of Cowan in view of Takao as suggested by the Examiner.

Accordingly, and based upon the above, it is respectfully submitted that claims 4, 8, 14, and 18 are allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because:

> "[T]he prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re* Vaeck, 947 F2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991)

The Examiner additionally stated that

> "Further, Takao teaches that the addition of parametric testing system is advantageous because it test [sic] wafers in the process for manufacturing semiconductor circuit devices. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Cowan by adding parametric test structure as taught by Takao in order to test wafers in the process for manufacturing semiconductor circuit devices."

However, the Examiner has not shown or cited a specific section in either Cowan or Takao that would support the above statement. Thus, no motivation has been presented for a person of ordinary skill in the art to attempt the suggested combination. It is not sufficient

that the proposed combination, if feasible, might be beneficial. Rather, it is necessary, as explained in *In re* Sang-Su Lee, 277 F.3d 1338, 61 USPQ2d 1430 (Fed. Cir. 2002), that there be a specific suggestion in one of the references to make the combination. In *In re* Sang-Su Lee, the Court held that the conclusion of obviousness may not be made from common knowledge and common sense of a person of ordinary skill in the art without any *specific* hint or suggestion in a particular reference.

Inasmuch as the Examiner has not cited in either reference any such specific hint or suggestion for the combination, the rejection based upon the assumed benefits of the hypothetical combination of Cowan in view of Takao cannot be maintained, and claims 4, 8, 14, and 18 are accordingly believed to be allowable thereover. Allowance thereof is therefore respectfully requested on this ground as well.

Regarding claims 5, 9, 15, and 19, these dependent claims depend respectively from claims 4, 8, 14, and 18 and are believed to be allowable since they contain all the limitations set forth therein and additionally claim non-obvious combinations thereof. Allowance of claims 5, 9, 15, and 19 is therefore respectfully requested on this ground as well because of *In re* Vaeck, *supra*.

The Applicants also respectfully traverse the rejection of claims 5, 9, 15, and 19 on the grounds that the Applicants' claimed combinations would be patentable over Cowan in view of Takao since the Applicants' claimed combinations, as exemplified in claim 5, includes the limitation not disclosed in either Cowan or Takao of:

using the parametric test structure to adjust the offset pattern of the contacts

The Examiner states in the Office Action:

> "...Cowan... does not disclose means for using the parametric test structure as claimed. Takao discloses [Fig. 6] a tester (tester 3) for failure analysis of small contacts in integrated circuits (IC wafer 2), comprising: a plurality of opposing electrical contact arrays (wafer prober 5), a parametric test structure (parametric testing system 1) for testing the opposing contacts and means (computer 6A) for using the parametric test structure (1) to adjust the offset pattern of the contacts"

However, Takao does not teach or suggest "means (computer 6A) for using the parametric test structure (1) to adjust the offset pattern of the contacts", but at column 1, lines 24–25, teaches:

> "a computer 6A for controlling the tester body 3 and wafer prober 5 and processing measured data"

The above shows that Takao does not teach or suggest using the parametric test structure to adjust the offset pattern of the contacts, and could not provide this teaching for a combination with Cowan.

Accordingly, neither Cowan nor Takao provides using the parametric test structure to adjust the offset pattern of the contacts, and there is thus no teaching, suggestion, or motivation in either of these references for the combination of Cowan in view of Takao as suggested by the Examiner.

Accordingly, and based upon the above, it is respectfully submitted that claims 5, 9, 15, and 19 are allowable under 35 U.S.C. §103(a) as being unobvious at the time the invention was made to a person having ordinary skill in the art because of *In re* Vaeck, *supra*.

The Examiner additionally stated that

> "Further, Takao teaches that the addition of means for using parametric testing system is advantageous because it test [sic] wafers in the process for manufacturing semiconductor circuit devices and controls the tester while processing measured data. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to modify the apparatus of Cowan by adding parametric test structure as taught by Takao in order to test wafers in the process for manufacturing semiconductor circuit devices and controls the tester while processing measured data."

However, the Examiner has not shown or cited a specific section in either Cowan or Takao that would support the above statement. Thus, no motivation has been presented for a person of ordinary skill in the art to attempt the suggested combination. *In re* Sang-Su Lee, *supra*.

Accordingly, allowance of claims 4, 5, 8, 9, 14, 15, 18, and 19 is respectfully requested.

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Conclusion

In view of the above, it is submitted that the claims are in condition for allowance and reconsideration of the rejections is respectfully requested. Allowance of claims 1–20 at an early date is solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including any extension of time fees, to Deposit Account No. 01-0365 and please credit any excess fees to such deposit account.

Respectfully submitted,

William D. Zahrt II
Registration No. 26,070

The Law Offices of Mikio Ishimaru
333 W. El Camino Real, Suite 330
Sunnyvale, CA 94087
Telephone: (408) 738-0592
Fax: (408) 738-0881
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